



Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT****Complete if Known**

Application No.	10/733,153
Filing Date	December 10, 2003
First Named Inventor	Donald E. Steiss
Art Unit	2181
Examiner Name	William M. Treat
Attorney Docket Number	22347-08260 (Seq. No. 8116)

Sheet	1	of	1
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U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document No. Number - Kind Code ² (if known)	Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
WMT	A1	US-5,881,277	03-09-1999	Bondi et al.
	A2	US-5,991,792	11-23-1999	Nageswaran
	A3	US-6,785,890	08-31-2004	Kalafatis et al.
	A4	US-6,792,446	09-14-2004	Merchant et al.
	A5	US-6,889,319	05-03-2005	Rodgers et al.
	A6	US-7,051,329	05-23-2006	Boggs et al.
	A7	US-2003/0037228	02-20-2003	Kelsey et al.
	A8	US-2003/0163675	08-28-2003	Bennett et al.
WMT	A9	US- 2003/0163589	08-28-2003	Bunce et al.

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Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ - Number ⁴ Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T ⁶

OTHER REFERENCES - NON-PATENT LITERATURE DOCUMENTS

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Examiner Signature	W. TREAT	Date Considered	3/3/07
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Examiner
Signature

W. TREAT

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WMT	C2	Boothe, B. and Ranade, A. G., "Improved Multithreading Techniques for Hiding Communication Latency in Multiprocessors," ACM 1992, pp. 214-223.	

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	C4	Tullsen, D. M. et al., "Exploiting Choice: Instruction Fetch and Issue on an Implementable Simultaneous Multithreading Processor," Proc. Of the 23 rd ISCA, May 1996, 12 pages.	
↓	C5	Tullsen, D. M. et al., "Simultaneous Multithreading: Maximizing On-Chip Parallelism," Proc. Of the 22 nd ISCA, June 1995, 12 pages.	
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Examiner Signature	W. TREAT	Date Considered	3/3/67
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